REMARKS

Claims 12-31 are pending in the present application. Claims 12, 17, 22 and 27 have been amended.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document in parent application Serial No. 09/497,684.

Specification

The Examiner has required amendment of the title to be more clearly indicative of the invention to which the claims are directed. The title has been amended as "SEMICONDUCUCTOR DEVICE INCLUDING A PROTECTIVE BACKING RESIN LAYER", as suggested by the Examiner.

Claim Rejections-35 U.S.C. 102

Claims 12-15, 17-20, 22-25 and 27-30 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Elenius et al. reference (U.S. Patent No. 6,441,487). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

Initially, since the effective U.S. filing date of the present application is February

4, 2000, it would appear that the Elenius et al. reference does not qualify as statutory prior art under the provisions of 35 U.S.C. 102(b). Presumably, this rejection should be considered under 35 U.S.C. 102(e). The Examiner is respectfully requested to clarify this point.

The semiconductor device of claim 12 includes in combination a semiconductor element; an electrode; a wiring portion; a conductive post; a resin layer; an external connection and a protective layer, "wherein an end portion of the protective layer is aligned with both an end portion of the semiconductor element and an end portion of the resin layer, and wherein the end portions of the protective layer, the semiconductor element and the resin layer define an outer edge of the semiconductor device". Applicant respectfully submits that the Elenius et al. reference does not disclose these features.

As relied upon by the Examiner, Fig. 2 of the Elenius et al. reference includes a second passivation layer 32 formed at front surface 12 of semiconductor wafer 14, and protective coating 34 formed at a rear surface 16 of semiconductor wafer 14. However, as described in column 5, lines 48-50 of the Elenius et al. reference, Fig. 2 is a cross-sectional view of **a portion** of a semiconductor wafer used to form the chip scale packaged integrated circuit shown in Fig. 1.

Accordingly, Fig. 2 of the Elenius et al. reference merely shows a part or portion of the chip scale packaged integrated circuit of Fig. 1. That is, Fig. 2 is merely a cross-sectional view, and does not show the whole area of the chip scale packaged integrated

circuit of Fig. 1 of the Elenius et al. reference. In Fig. 1 of the Elenius et al. reference, the outer perimeter of the chip scale packaged integrated circuit 8 is illustrated by reference numeral 21. However, Fig. 2 of the Elenius et al. reference does not specifically show any portion corresponding to the outer perimeter 21 shown in Fig. 1. There is no description in the Elenius et al. reference that the end portions shown in Fig. 2 corresponds to outer perimeter 21 of Fig. 1. Accordingly, the Elenius et al. reference does not specifically show or disclose end portions of a protective layer, a semiconductor element and a resin layer that define an outer edge of a semiconductor device, as would be necessary to meet the features of claim 12. Applicant therefore respectfully submits that the semiconductor device of claim 12 distinguishes over the Elenius et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 12-15, is improper for at least these reasons.

The semiconductor device of claim 17 features in combination "wherein a side surface of the semiconductor element is exposed from the resin layer and the protective layer, wherein an end portion of the protective layer is aligned with both the exposed side surface of the semiconductor element and an end portion of the resin layer, and wherein the end portions of the protective layer and the resin layer, and the exposed side surface of the semiconductor element define an outer edge of the semiconductor device".

Applicant respectfully submits that the Elenius et al. reference does not disclose these features, because Fig. 2 merely shows a cross-sectional view of a portion of the

chip scale packaged integrated circuit of Fig. 1. Applicant therefore respectfully submits that the semiconductor device of claim 17 distinguishes over the Elenius et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 17-20, is improper for at least these reasons.

The semiconductor device of claim 22 features in combination "wherein only a side surface of the semiconductor element is exposed from the resin layer and the protective layer, wherein an end portion of the protective layer is aligned with both the side surface of the semiconductor element and an end portion of the resin layer, and wherein the end portions of the protective layer and the resin layer, and the side surface of the semiconductor element define an outer edge of the semiconductor device".

Applicant respectfully submits that the Elenius et al. reference as relied upon by the Examiner does not disclose the above noted features, because Fig. 2 merely shows a cross-sectional view of a portion of the chip scale packaged integrated circuit of Fig. 1. Applicant therefore respectfully submits that the semiconductor device of claim 22 distinguishes over the Elenius et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 22-25, is improper for at least these reasons.

The semiconductor device of claim 27 features in combination "wherein a side surface of the protective layer is in a same plane with both a side surface of the semiconductor element and a side surface of the resin layer, and wherein the side

surfaces of the protective layer, the semiconductor element and the resin layer define an outer edge of the semiconductor device".

Applicant respectfully submits that the Elenius et al. reference does not disclose these features, because Fig. 2 merely illustrates a cross-sectional view of a portion of the chip scale packaged integrated circuit of Fig. 1. Applicant therefore respectfully submits that the semiconductor device of claim 27 distinguishes over the Elenius et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 27-30, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 16, 21, 26 and 31 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Elenius et al. reference, in further view of the Kim et al. reference (U.S. Patent No. 6,004,867). Applicant respectfully submits that the Kim et al. reference as secondarily relied upon does not overcome the above noted deficiencies of the primarily relied upon Elenius et al. reference. Applicant therefore respectfully submits that claims 16, 21, 26 and 31 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the

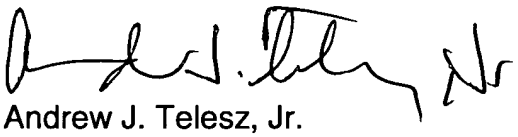
corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0720
Facsimile No.: (571) 283-0740